REMARKS

Claims 1-10 remain pending in this application with claim 10 being amended by this response.

Objection to the Abstract

The Abstract is objected to as being a duplication of claim 1 and not being in narrative form. The Abstract has been amended in accordance with the comments in the Office Action to be in the proper form and include the proper content of an Abstract. In view of the amendments to the Abstract, it is respectfully submitted that this objection is satisfied and should be withdrawn.

Rejection of claim 10 under 35 U.S.C. 112, second paragraph

Claim 10 is rejected under 35 U.S.C. 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention.

Claim 10 has been amended for purposes of clarity. It is respectfully submitted that the term "apparatus" is clear from the claim. Furthermore, it is respectfully submitted that an apparatus for reading from a recording medium and writing to a recording medium is clear to one skilled in the art. In view of the amendments to claim 10, it is respectfully submitted that this rejection is satisfied and should be withdrawn.

Rejection of claims 1-8 and 10 under 35 U.S.C. 103(a)

Claims 1-8 and 10 are rejected under 35 U.S.C. 103(a) as being unpatentable over Demura (U.S. Publication No. 2002/0099996) in view of Greenblat (U.S. Publication No. 2003/0212830).

The present claimed invention provides a method and apparatus for error correction of an encoded data stream.. The data stream is saved in an input buffer and a first correction process is performed on-the-fly in the input buffer. The data is transferred to an external DRAM after correction. The data is then copied from the external DRAM to an embedded SRAM. A multipass correction is started in the embedded SRAM and the corrected data is copied back from the embedded SRAM to the external DRAM after the multipass correction. Independent Claims 1 and 8 include similar features to those discussed above and thus, all arguments presented below apply to each of these claims.

The present invention provides a method for error correction of an encoded data stream including performing a first correction process on-the-fly in the input buffer (SRAM). This provides the advantage of performing the correction process in the fast internal SRAM while input/output streaming is performed in the comparatively slower external DRAM. As a result, the number of random accesses to the external DRAM is reduced. After the first correction process, data is streamed to the external DRAM. After gathering a full ECC block in the external DRAM, the data is then streamed to the internal SRAM where the ECC block is corrected using a multipass correction method. The data is then streamed back to the DRAM. The overall correction process is sped up, and the size of the internal SRAM is reduced by the present claimed invention. Additionally, the internal SRAM correction simplifies the hardware complexity during the correction process.

Demura describes a method of detecting and correcting errors and erasures in ECC-coded data arrays for DVD systems. The received data blocks are stored in main DRAM memory 12. A portion of the received data blocks are copied from main DRAM memory 12 to a buffer SRAM memory 13 in order to calculate correction bit patterns (See Demura, paragraph [0055]). SRAM memory 13 also includes sections 14 and 15 for storing rows and columns of data blocks, as well as sections 14A and 15A for storing dense maps to identify error locations and correction bit patterns. The correction is effectuated as indexed by the dense map (paragraph [0013]).

Unlike the present claimed invention, buffer memory sections 14, 15, 14A, and 15A of Demura do not include corrected data blocks in any method step. The data is also not

corrected in the SRAM. Instead, data is corrected in the DRAM based on dense maps stored in the SRAM (Fig. 6, step 49, paragraph [0055]). As a result, erroneous data is identified, the address of the erroneous data in main DRAM memory 12 is calculated, and the erroneous data is corrected by using the correction bit pattern. The data is then stored in main DRAM memory 12 (see Demura, paragraph [0055]). Therefore, Demura neither discloses nor suggests "performing a first correction process on-the-fly in the input buffer" as recited in the present claimed invention.

Greenblat describes data communication networks and, more particularly, receiving and transmitting systems, including ATM and other types of communications platforms including such components as communications processors, packet processors, network processors, DMA's, FPGA's and other devices and peripheral devices. Greenblat is not concerned with nor even mentions correction of erroneous data blocks on-the-fly in the fast SRAM. Therefore, Greenblat, similarly to Demura, neither discloses nor suggests "performing a first correction process on-the-fly in the input buffer" as recited in the present claimed invention.

Additionally, as the individual systems of Demura and Greenblat neither disclose nor suggest "performing a first correction process on-the-fly in the input buffer" as recited in the present claimed invention, it is respectfully submitted that any combination of Demura and Greenblat cannot disclose this feature. Thus, the combination of Demura and Greenblat as suggested in the Office Action neither discloses nor suggests "performing a first correction process on-the-fly in the input buffer" as recited in claim 1 of the present invention. Independent claim 8 includes a similar feature and thus, it is respectfully submitted that claim 8 is also patentable.

In view of the above remarks, it is respectfully submitted that there is no 35 USC 112 enabling disclosure in Demura or Greenblat when taken alone or in combination that would make the present invention as claimed in claims 1 and 8 unpatentable. As claims 2-7 and 10 are dependent on claims 1 and 8 respectively, it is respectfully submitted that these claims are also patentable for the same reasons as claims 1 and 8. Therefore, in view of the above

remarks, it is further respectfully submitted that this rejection is satisfied and should be withdrawn.

Having fully addressed the Examiner's rejections, it is believed that, in view of the amendments and remarks, this application stands in condition for allowance. Accordingly then, reconsideration and allowance are respectfully solicited. If, however, the Examiner is of the opinion that such action cannot be taken, the Examiner is invited to contact the applicant's attorney at the phone number below, so that a mutually convenient date and time for a telephonic interview may be scheduled.

No fee is believed due with this response. However, if a fee is due, please charge the fee to Deposit Account 07-0832.

Respectfully submitted,
Stefan Muller et al.

By: _____
Jack Schwartz
Reg. No. 34,721
Tel. No. (609)734-6866

Thomson Licensing, LLC
Patent Operations
PO Box 5312
Princeton, NJ 08543-5312
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Jack Schwartz
Reg. No. 34,721